UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/699,047	10/30/2003	Ji-young Kim	9898-300	1200

20575 7590 03/01/2006

MARGER JOHNSON & MCCOLLOM, P.C.
210 SW MORRISON STREET, SUITE 400
PORTLAND, OR 97204

EXAMINER	
DUONG, KHANH B	

ART UNIT	PAPER NUMBER
2822	

DATE MAILED: 03/01/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/699,047	KIM, JI-YOUNG	
	Examiner	Art Unit	
	Khanh B. Duong	2822	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *23 November 2005*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *8-15 and 17-24* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *8-15 and 17-24* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date 9/23/05
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Response to Amendment

This Office Action is in response to the amendment filed on November 23, 2005.

Accordingly, claims 8, 10, 11, 14, 15 and 20 were amended, and new claims 23 and 24 were added.

Currently, claims 8-15 and 17-24 remain pending.

Information Disclosure Statement

The information disclosure statement (IDS) filed September 23, 200 5 has not been considered by the Examiner because it is a duplicate of the IDS filed February 22, 2005 (see attached copy).

Response to Arguments

Applicant's arguments with respect to the amended claims have been considered but are moot in view of the new ground(s) of rejection.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

Claims 8, 11-13, 15, 17, 19, 23 and 24 are rejected under 35 U.S.C. 102(e) as being anticipated by Weis (US 2002/0196651 A1).

Re claim 8, Weis expressly discloses in FIG. 2 a method of forming a MOSFET having a recessed channel, comprising: forming a trench in a semiconductor substrate; forming a gate dielectric layer (32 and 36) on an inner wall and a bottom of said trench; sequentially forming a gate conductive layer (34, 40 and 42) and a capping layer 44 on the gate dielectric layer so as to fill the trench; forming a gate electrode (34, 40, 42 and 44) having a first portion (part of 34 above the substrate) which rises over the semiconductor substrate and a second portion (part of 34 in the substrate) filling the trench by patterning the capping layer 44 and the gate conductive layer (34, 40 and 42), wherein the first portion has a smaller width than that of the second portion; and forming a source/drain region 38 by implanting impurity ions into the semiconductor substrate on both sides of the gate electrode.

Re claim 11, Weis discloses the gate dielectric layer (32 and 36) is formed of silicon oxide [see page 2, paragraphs 0023 and 0024].

Re claim 12, Weis discloses the gate conductive layer comprises a conductive polysilicon layer 34 that fills the trench and a metal layer (40 and 42) formed on the conductive polysilicon layer 34 [see pages 2-3, paragraph 0024].

Re claim 13, Weis discloses in FIGs. 4a and 4b forming a sacrificial (collar) oxide layer 30 by thermally oxidizing the semiconductor substrate; and removing the sacrificial oxide layer 30 using a wet etch process [see page 3, paragraph 0028].

Re claims 15 and 17, Weis expressly discloses in FIG. 2 forming spacers (parts of 44 and 46) on sidewalls of the gate electrode (34, 40, 42 and 44), wherein a portion of the spacers (parts of 46) are extended into the semiconductor substrate.

Re claim 19, Weis expressly discloses in FIG. 2 the source/drain region 38 is shallower than the bottom of the trench.

Re claims 23 and 24, Weis expressly discloses in FIG. 2 the width of the first portion of the gate electrode 34 plus the spacers 46 is less than that of the second portion of the gate electrode 34, and that the spacers 46 extend the entire height of the first portion of the gate electrode.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

Claims 20 and 22 are rejected under 35 U.S.C. 103(a) as being unpatentable over Weis in view of Cha (KR 2001-64328).

Weis discloses in FIG. 2 a method of forming a MOSFET having a recessed channel, comprising: forming a trench in a semiconductor substrate using a etch process; forming a gate dielectric layer (32 and 36) on an inner wall and a bottom of said trench; sequentially forming a

gate conductive layer 34 and a capping layer 44 on the gate dielectric layer so as to fill the trench; forming a gate electrode having a first portion (portion of 34 over the substrate) which rises over the semiconductor substrate and a second portion (in the substrate) filling the trench by patterning the capping layer 44 and the gate conductive layer 34, wherein the first portion has a smaller width than that of the second portion; forming spacers 46 on the sidewalls of the gate electrode 34, wherein a portion of the spacers 46 are extended into the semiconductor substrate; and forming a source/drain region 38 by implanting impurity ions into the semiconductor substrate on both sides of the gate electrode 34, and wherein forming the gate electrode 34 comprises recessing the gate conductive layer that fills the trench to a depth of approximately 70 nm (700 Angstroms) from a top surface of the semiconductor substrate by inherently adjusting etching time.

Re claim 20, Weis discloses recessing recessing the gate conductive layer that fills the trench to a depth of approximately 70 nm (700 Angstroms), instead of 500 Angstroms or less.

However, it would have been obvious to a person of ordinary skill in the art at the time the invention was made to optimize and select an appropriate depth. The selection of parameters such as energy, power, concentration, temperature, time, depth, thickness, etc., would have been obvious and involve routine optimization which has been held to be within the level of ordinary skill in the art. "Normally, it is to be expected that a change in temperature, or in concentration, or in both, would be an unpatentable modification. Under some circumstances, however, changes such as these may be impart patentability to a process if the particular ranges claimed produce new and unexpected result which is different in kind and not merely degree from results of prior art ... such ranges are termed 'critical ranges' and the applicant has the burden of

proving such criticality ... More particularly, where the general conditions of a claim are disclosed in the prior art, it is not inventive to discover the optimum or workable ranges by routine experimentation". *In re Aller*, 105 USPQ 233, 235 (CCPA 1955). See also MPEP 2144.05.

Re claim 22, Weis expressly discloses in FIG. 2 the source/drain region 38 is shallower than the bottom of the trench.

Claim 21 is rejected under 35 U.S.C. 103(a) as being unpatentable over Weis in view of Ishikawa et al. (US 6,482,701).

Re claim 21, Weis fails to disclose the specific depth of the trench of about 1000 Angstroms to about 1500 Angstroms and further etching the trench by about 100 Angstroms to about 200 Angstroms using a chemical dry etch process.

Ishikawa teaches in FIGs. 1A-1D a rectangular trench 5 is formed to a depth of about 4 to 6 micrometers (40,000 to 60,000 angstroms) and is further etched to about 0.10 to 0.20 micrometers (1,000 to 2,000 angstroms) using a chemical dry etch process.

It would have been obvious to a person of ordinary skill in the art at the time the invention was made to optimize and select appropriate depths for the trench. The selection of parameters such as energy, power, concentration, temperature, time, depth, thickness, etc., would have been obvious and involve routine optimization which has been held to be within the level of ordinary skill in the art. "Normally, it is to be expected that a change in temperature, or in concentration, or in both, would be an unpatentable modification. Under some circumstances, however, changes such as these may be impart patentability to a process if the particular ranges claimed produce new and unexpected result which is different in kind and not merely degree

from results of prior art ... such ranges are termed 'critical ranges' and the applicant has the burden of proving such criticality ... More particularly, where the general conditions of a claim are disclosed in the prior art, it is not inventive to discover the optimum or workable ranges by routine experimentation". *In re Aller*, 105 USPQ 233, 235 (CCPA 1955). See also MPEP 2144.05.

Claims 8, 11, 14, 15, 17 and 19 are rejected under 35 U.S.C. 103(a) as being unpatentable over Lu in view of Cha.

Lu discloses in FIGs. 3A-6B a method of forming a MOSFET having a recessed channel, comprising: forming a trench 14 in a semiconductor substrate 8, forming a gate dielectric layer 20 on an inner wall and a bottom of said trench 14; sequentially forming a gate conductive layer 22 and a capping layer 24 on the gate dielectric layer 20 so as to fill the trench 14; forming a gate electrode 28 having a first portion which rises over the semiconductor substrate 8 and a second portion filling the trench 14 by patterning the capping layer 24 and the gate conductive layer 22, wherein the first portion has a larger width than that of the second portion [see illustration of FIG. 6B below]; and forming a source/drain region 30 by implanting impurity ions into the semiconductor substrate 8 on both sides of the gate electrode 28.

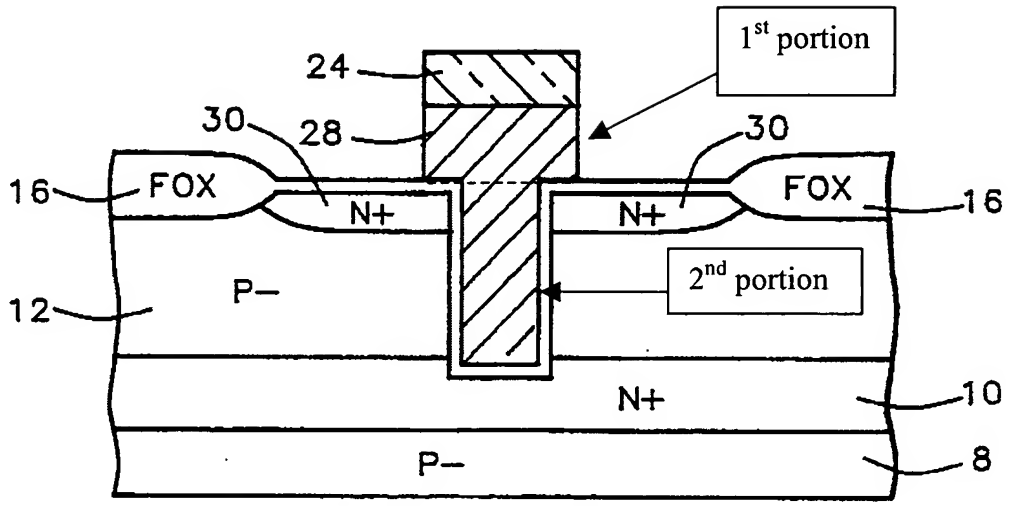

FIG. 6B

Re claim 8, Lu fails to disclose the width of the first portion of the gate electrode being smaller than that of the second portion.

Cha expressly teaches in FIG. 1d the width of the first portion (above the substrate) of the "inverse T-shaped gate electrode" being smaller than that of the second portion (in the substrate) for the purpose of preventing a short channel effect and a hot carrier effect [see English Abstract].

Since Lu and Cha are from the same field of endeavor, the purpose disclosed by Cha would have been recognized in the pertinent prior art of Lu.

Therefore, it would have been obvious to a person of ordinary skill in the art at the time the invention was made to modify the method disclosed by Lu as taught by Cha because of the desirability to prevent a short channel effect and a hot carrier effect.

Re claim 11, Lu discloses the gate dielectric layer 20 is formed of silicon oxide [see col. 4, lines 56-59].

Re claims 14 and 17, Lu fails to disclose recessing the gate conductive layer that fills the trench to a depth of 500 Angstroms or less from the surface of the semiconductor substrate by adjusting an etching time, and forming spacers on the sidewalls of the gate electrode, wherein a potion of the spacers are extended into the semiconductor substrate.

Cha expressly teaches in figs. 1a-1d recessing the gate conductive layer 26 that fills the trench 22 to a certain depth from the surface of the semiconductor substrate 10 by inherently adjusting an etching time, and forming spacers 32 on the sidewalls of the gate electrode 26', wherein a potion of the spacers 32 are extended into the semiconductor substrate 10 [see English Abstract].

Since Lu and Cha are from the same field of endeavor, the purpose disclosed by Cha would have been recognized in the pertinent prior art of Lu.

Therefore, it would have been obvious to a person of ordinary skill in the art at the time the invention was made to modify the method disclosed by Lu as taught by Cha for the purposes of insulating the gate electrode and preventing a short channel effect and a hot carrier effect.

Furthermore, it would have been obvious to a person of ordinary skill in the art at the time the invention was made to optimize and select an appropriate depth and time for the etching process. The selection of parameters such as energy, power, concentration, temperature, time, depth, thickness, etc., would have been obvious and involve routine optimization which has been held to be within the level of ordinary skill in the art. "Normally, it is to be expected that a change in temperature, or in concentration, or in both, would be an unpatentable modification.

Under some circumstances, however, changes such as these may be impart patentability to a process if the particular ranges claimed produce new and unexpected result which is different in kind and not merely degree from results of prior art ... such ranges are termed 'critical ranges' and the applicant has the burden of proving such criticality ... More particularly, where the general conditions of a claim are disclosed in the prior art, it is not inventive to discover the optimum or workable ranges by routine experimentation". *In re Aller*, 105 USPQ 233, 235 (CCPA 1955). See also MPEP 2144.05.

Re claim 15, Lu expressly discloses in FIG. 8B forming spacers 32 on sidewalls of the gate electrode 28.

Re claim 19, Lu expressly discloses in FIG. 6B the source/drain region 30 is shallower than the bottom of the trench 14.

Claims 9, 10 and 18 are rejected under 35 U.S.C. 103(a) as being unpatentable over Lu and Cha as applied to claims 8, 11, 15 and 19 above, and further in view of Ishikawa.

Re claims 9 and 18, Lu discloses forming a rectangular trench 14 in the semiconductor substrate 8 using an anisotropic etch process, but fails to disclose further etching the trench using a chemical dry etching to cause the trench to have a round profile. Cha also fails to teach such feature.

Ishikawa et al. ("Ishikawa") teaches in FIGs. 1A-1D making a trench 5, which was etched using an anisotropic (RIE) etch process, have a round profile by further etching the trench 5 using a chemical dry etching [see col. 3, line 26 to col. 4, line 60].

Since Lu, Cha and Ishikawa are from the same field of endeavor, the purpose disclosed by Ishikawa would have been recognized in the pertinent prior art of Lu and Cha.

Therefore, it would have been obvious to a person of ordinary skill in the art at the time the invention was made to modify the combined method of Lu and Cha in the manner as taught by Ishikawa, since Ishikawa states at column 1, lines 35-48 that such modification would reduce not only deterioration in film quality or thinning of a gate oxide, but also electric field at the corner of a bottom portion of the trench. As a result, a withstand voltage breakdown would be minimized at such corner.

Re claim 10, Lu discloses the rectangular trench is formed to a depth of about 0.1 to 0.7 micrometers (1,000 to 7,000 angstroms). Ishikawa discloses the rectangular trench is formed to a depth of about 4 to 6 micrometers (40,000 to 60,000 angstroms) and is further etched to about 0.10 to 0.20 micrometers (1,000 to 2,000 angstroms) using a chemical dry etch process. However, both Lu and Ishikawa fail to disclose the specific ranges of depths as claimed.

It would have been obvious to a person of ordinary skill in the art at the time the invention was made to optimize and select appropriate depths for the trench. The selection of parameters such as energy, power, concentration, temperature, time, depth, thickness, etc., would have been obvious and involve routine optimization which has been held to be within the level of ordinary skill in the art. "Normally, it is to be expected that a change in temperature, or in concentration, or in both, would be an unpatentable modification. Under some circumstances, however, changes such as these may be impart patentability to a process if the particular ranges claimed produce new and unexpected result which is different in kind and not merely degree from results of prior art ... such ranges are termed 'critical ranges' and the applicant has the burden of proving such criticality ... More particularly, where the general conditions of a claim are disclosed in the prior art, it is not inventive to discover the optimum or workable ranges by

routine experimentation". *In re Aller*, 105 USPQ 233, 235 (CCPA 1955). See also MPEP 2144.05.

Claim 12 is rejected under 35 U.S.C. 103(a) as being unpatentable over Lu and Cha as applied to claims 8, 11, 15 and 19 above, and further in view of Durcan et al. (US 6,780,732).

Re claim 12, Lu fails to disclose forming a gate conductive layer comprising a conductive polysilicon layer that fills the trench and a metal layer on the conductive polysilicon layer. Cha also fails to teach such feature.

Durcan et al. ("Durcan") teaches in FIG. 20 forming a gate conductive layer 90 comprising a conductive polysilicon layer 33 that fills the trench 20 and a metal layer 37 on the conductive polysilicon layer 33 [see col. 5, lines 13-54].

Since Lu, Cha and Durcan are from the same field of endeavor, the purpose disclosed by Durcan would have been recognized in the pertinent prior art of Lu and Cha.

Therefore, it would have been obvious to a person of ordinary skill in the art at the time the invention was made to modify the combined method of Lu and Cha as taught by Durcan, since Durcan states at column 5, lines 23-29 that such modification would form low resistance and low resistivity conductive regions on top of the polysilicon gates 33.

Claim 13 is rejected under 35 U.S.C. 103(a) as being unpatentable over Lu and Cha as applied to claims 8, 11, 15 and 19 above, and further in view of Chang et al. (US 6,509,233).

Re claim 13, Lu fails to disclose forming a sacrificial oxide layer in the trench by thermally oxidizing the semiconductor substrate; and removing the sacrificial oxide layer using a wet etch process. Cha also fails to teach such feature.

Chang et al. ("Chang") suggests forming a sacrificial oxide layer in a trench by thermally oxidizing the semiconductor substrate; and removing the sacrificial oxide layer using a wet etch process to remove defects created by a prior etch (RIE) process to form the trench [see col. 3, lines 25-35].

Since Lu, Cha and Chang are from the same field of endeavor, the purpose disclosed by Chang would have been recognized in the pertinent prior art of Lu and Cha.

Therefore, it would have been obvious to a person of ordinary skill in the art at the time the invention was made to modify the combined method of Lu and Cha as suggested by Chang because of the desirability to remove defects created by a prior etch process to form the trench.

Conclusion

Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event,

however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Khanh B. Duong whose telephone number is (571) 272-1836. The examiner can normally be reached on 10:00-6:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Zandra Smith, can be reached on (571) 272-2429. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

KBD

Zandra V. Smith
Supervisory Patent Examiner
17 Feb. 2006